ISO8200AQ

Galvanic isolated octal high side smart power solid state relay with SPI interface

Datasheet - Production data

TFQFPN32

Features

- V_{demag} = V_{CC} - 45 V (per channel)
- $R_{DS(on)}$ = 0.120 Ω (per channel)
- I_{OUT} = 0.7 A (per channel)
- V_{CC} = 45 V
- SPI interface with daisy chaining
- 5 V and 3.3 V TTL/CMOS & µC compatible I/Os
- Common output enable/disable pin
- Fast demagnetization of inductive loads
- Reset function for IC outputs disable
- Very low supply current
- Undervoltage shutdown with auto restart and hysteresis
- Short-circuit protection
- Per-channel overtemperature protection
- Thermal independence of separate channels
- Case overtemperature protection
- Loss of Ground and Supply protections
- Overvoltage protection (V_{CC} clamping)
- Common OVT fault open drain output
- Power GOOD open drain output
- High common mode transient immunity
- ESD protection
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5 and IEC 61000-4-8
- UL1577 certified

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Drivers for all type of loads (resistive, capacitive, inductive)

Description

The ISO8200AQ is a galvanic isolated 8-channel driver featuring a very low supply current. It contains 2 independent galvanic isolated voltage domains (V_{CC} and V_{DD} for the Process and Control Logic stages, respectively). The IC is intended for driving any kind of load with one side connected to ground.

The Control Logic Stage features an 8-bit Output Status Register (where the µC sets the status ON/OFF of the output channels in the Process Stage) and an 8-bit Fault Register (where the OVT faults of each channel are stored). The two stages communicate through the galvanic isolation channel by an ST proprietary protocol.

Active channel current limitation (OVL) combined with thermal shutdown (OVT), independent for each channel, protects the device against overload and overtemperature.

Additional embedded functions are: loss of ground protection, V_{CC} and V_{DD} UVLOs (with hysteresis), watchdog and V_{CC} Power GOOD.

An internal circuit provides an OR-wired not latched common ($\overline{\text{FAULT}}$) indicator signaling the channel OVT. The ($\overline{\text{PGOOD}}$) diagnostic pin is activated if V_{CC} goes below the power good internal threshold. Both ($\overline{\text{FAULT}}$) and ($\overline{\text{PGOOD}}$) pins are open drain, active low, fault indication pins.

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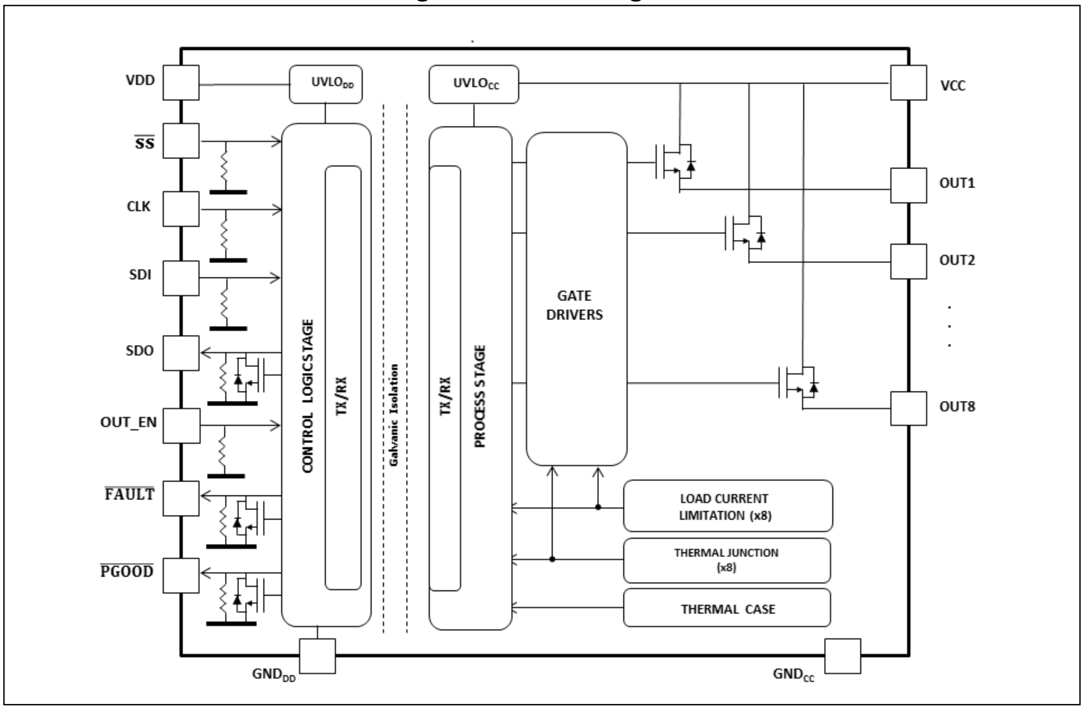
Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top through view)

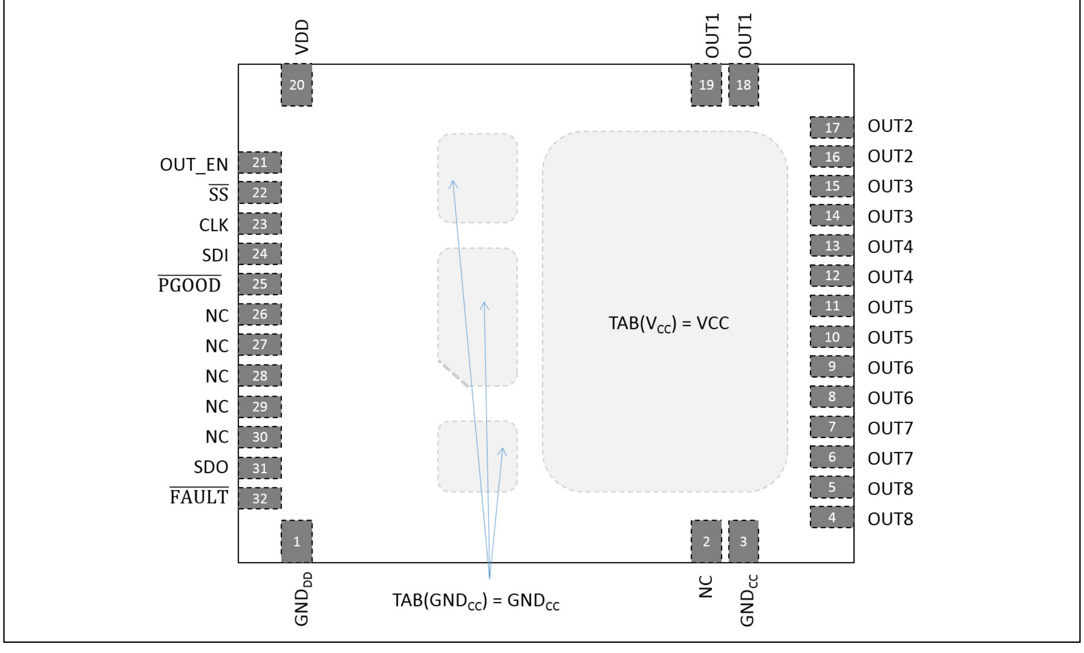


Table 1. Pin description

Pin	Name	Description
1	GND_{DD}	Input Control Logic Stage ground, negative logic supply
2	NC	Not connected
3	GND_{CC}	Output power ground
4	OUT8	Channel 8 power output
5	OUT8	
6	OUT7	Channel 7 power output
7	OUT7	
8	OUT6	Channel 6 power output
9	OUT6	
10	OUT5	Channel 5 power output
11	OUT5	
12	OUT4	Channel 4 power output
13	OUT4	
14	OUT3	Channel 3 power output
15	OUT3	
16	OUT2	Channel 2 power output
17	OUT2	

Table 1. Pin description (continued)

Pin	Name	Description
18	OUT1	Channel 1 power output
19	OUT1	
20	V_{DD}	Positive Control Logic Stage supply
21	OUT_EN	Output enable
22	$\overline{SS}$	Chip select
23	$\overline{CLK}$	Serial Clock Digital Input
24	SDI (MOSI)	SPI device Input
25	$\overline{PGOOD}$	Power Good diagnostic pin - active low
26	NC	Not connected
27	NC	Not connected
28	NC	Not connected
29	NC	Not connected
30	NC	Not connected
31	SDO (MISO)	SPI device Output
32	$\overline{FAULT}$	Common fault diagnostic pin - active low
TAB(V_{CC})	V_{CC}	Exposed tab internally connected to V_{CC}, positive Process Stage supply voltage
TAB(GND_{CC})	GND_{CC}	Exposed tab internally connected to GNDcc (ground of Process Stage)

3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Process Stage supply voltage	-0.3	+45	V
V_{DD}	Control Logic Stage supply voltage	-0.3	+6.5	V
V_{IN}	DC Input pins voltage (INx, SS, CLK, SDI, OUT_EN)	-0.3	+6.5	V
V_{FAULT}, V_{PGOOD}	$\overline{\text{FAULT}}$ and $\overline{\text{PGOOD}}$ pins voltage	-0.3	+6.5	V
I_{GNDdd}	DC digital ground reverse current		-25	mA
I_{OUT}	Channel Output Current (continuous)		Internally limited	A
I_{GNDcc}	DC power ground reverse current		-250	mA
I_{RX}	Single channel reverse output current (from OUTX pins to V_{CC})		-5	A
I_{RT}	Total reverse output current (from OUTX pins to V_{CC}) @ TAMB 25°C		-12	A
I_{IN}	DC Input pins current (INx, SS, CLK, SDI, OUT_EN)	-10	+10	mA
I_{FAULT}, I_{PGODD}	$\overline{\text{FAULT}}$ and $\overline{\text{PGOOD}}$ pins current	-10	+10	mA
V_{ESD}	Electrostatic discharge with Human Body Model (R = 1.5K Ω; C = 100 pF)		2000	V
EAS	Single pulse avalanche energy per channel not simultaneously @Tamb= 125 °C, I_{OUT} = 0.5 A		1.8	J
	Single pulse avalanche energy per channel, all channels driven simultaneously @Tamb= 125 °C, I_{OUT} = 0.5 A		0.35	
P_{TOT}	Power dissipation at T_c = 25 °C		Internally limited (1)	W
T_J	Junction operating temperature		Internally limited (1)	°C
T_{STG}	Storage temperature		-55 to 150	°C

1. Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous or repetitive operation of protection functions may reduce the IC lifetime.

4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction-to-case (1)	1	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient (2)	25	
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient (3)	15	

1. Rth between the die and the bottom case surface measured by cold plate as per JESD51.
2. JESD51-7.
3. IC mounted on the product evaluation board (FR4, 4 layers, 8 cm2 for each layer, copper thickness 35 mm).

5 Electrical characteristics

(10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C, unless otherwise specified.)

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC(THON)}$	V_{CC} undervoltage turn-on threshold			9.5	10.5	V
$V_{CC(THOFF)}$	V_{CC} undervoltage turn-off threshold		8	9		V
$V_{CC(HYS)}$	V_{CC} undervoltage hysteresis		0.25	0.5		V
$V_{CCclamp}$	Clamp on VCC pin	Iclamp = 20 mA	45	50	52	V
$V_{CC(PGON)}$	V_{CC} Power Good turn-on threshold	V_{DD} = 3.3 V, VCC increasing		17.5	18.4	V
$V_{CC(PGOFF)}$	V_{CC} Power Good turn-off threshold	V_{DD} = 3.3 V, VCC decreasing	15.2	16.5		V
$V_{CC(PG-HYS)}$	V_{CC} Power Good hysteresis			1		V
$R_{DS(ON)}$	ON state resistance	I_{OUT} = 0.5 A, T_J = 25 °C		0.12		Ω
		I_{OUT} = 0.5 A, T_J = 125 °C			0.24	
R_{PD}	Output pull-down resistor			210		kΩ
I_{CC}	Power supply current	All channels in OFF state All channels in ON state		5 9		mA
I_{LGND}	Ground disconnection output current	V_{CC} = VGND = 0 V V_{OUT} = -24 V			500	µA
$V_{OUT(OFF)}$	OFF state output voltage	Channel OFF and I_{OUT} = 0 A			1	V
$I_{OUT(OFF)}$	OFF state output current	Channel OFF and V_{OUT} = 0 V			5	µA

Table 5. Digital supply voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage range		2.75		5.5	V
$V_{DD(THON)}$	V_{DD} undervoltage turn-on threshold		2.55		2.75	V
$V_{DD(THOFF)}$	V_{DD} undervoltage turn-off threshold		2.45		2.65	V
$V_{DD(HYS)}$	V_{DD} undervoltage hysteresis		0.04	0.1		V
I_{DD}	V_{DD} supply current	V_{DD} = 5 V and SPI not transmitting		4.5	6	mA
		V_{DD} = 3.3 V and SPI not transmitting		4.4	5.9	mA

Table 6. Diagnostic pin and output protection function

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{FAULT}	$\overline{\text{FAULT}}$ pin open drain voltage output low	I_{FAULT} = 5 mA			0.4	V
I_{LFAULT}	$\overline{\text{FAULT}}$ output leakage current	V_{FAULT} = 5 V			1	µA
V_{PGOOD}	$\overline{\text{PGOOD}}$ pin open drain voltage output low	I_{PGOOD} = 5 mA			0.4	V
I_{LPGOOD}	$\overline{\text{PGOOD}}$ output leakage current	V_{PGOOD} = 5 V			1	µA
I_{PEAK}	Maximum DC output current before limitation	V_{CC} = 24 V R_{LOAD} = 0 Ω		1.6		A
I_{LIM}	Short-circuit current limitation		0.7	1.3	1.9	A
Hyst	ILIM tracking limits			0.3		A
T_{JSD}	Junction shutdown temperature		150	170		°C
T_{JR}	Junction reset temperature			150		°C
T_{HIST}	Junction thermal hysteresis			20		°C
T_{CSD}	Case shutdown temperature		115	130	145	°C
T_{CR}	Case reset temperature			110		°C
T_{CHYST}	Case thermal hysteresis			20		°C
V_{DEMAG}	Output voltage at turn-off	I_{OUT} = 0.5 A; ILOAD >= 1 mH	V_{CC}-45	V_{CC}-50	V_{CC}-52	V

Table 7. Power switching characteristics (V_{CC} = 24 V; -40°C < T_J < 125°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dV/dt(ON)	Turn-on voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω		5.6		V/µs
dV/dt(OFF)	Turn-off voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω		2.81		V/µs
td(ON)	Turn-on delay time (see *Figure 5*)	I_{OUT} = 0.5 A, resistive load 48 Ω		17	22	µs
td(OFF)	Turn-off delay time (see *Figure 5*)	I_{OUT} = 0.5 A, resistive load 48 Ω		22	40	µs
tf	Fall time (see *Figure 4*)	I_{OUT} = 0.5 A, resistive load 48 Ω		5		µs
tr	Rise time (see *Figure 4*)	I_{OUT} = 0.5 A, resistive load 48 Ω		5		µs
$t_{w(OUT\_EN)}$	OUT_EN pulse width (see *Figure 10*, *11*)	I_{OUT} = 0.5 A, resistive load 48 Ω	150			ns
$t_{p(OUT\_EN)}$	OUT_EN propagation delay (see *Figure 10*, *11*)	I_{OUT} = 0.5 A, resistive load 48 Ω		22	40	µs

Figure 3. RDS(on) measurement

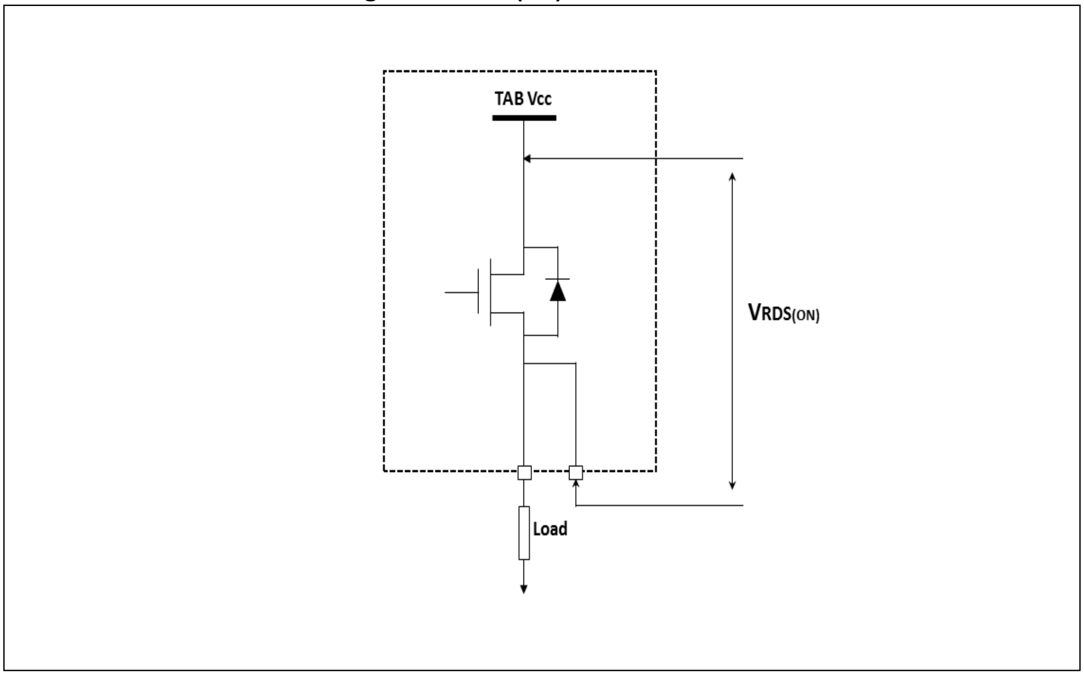


Figure 4. dV/dT definition

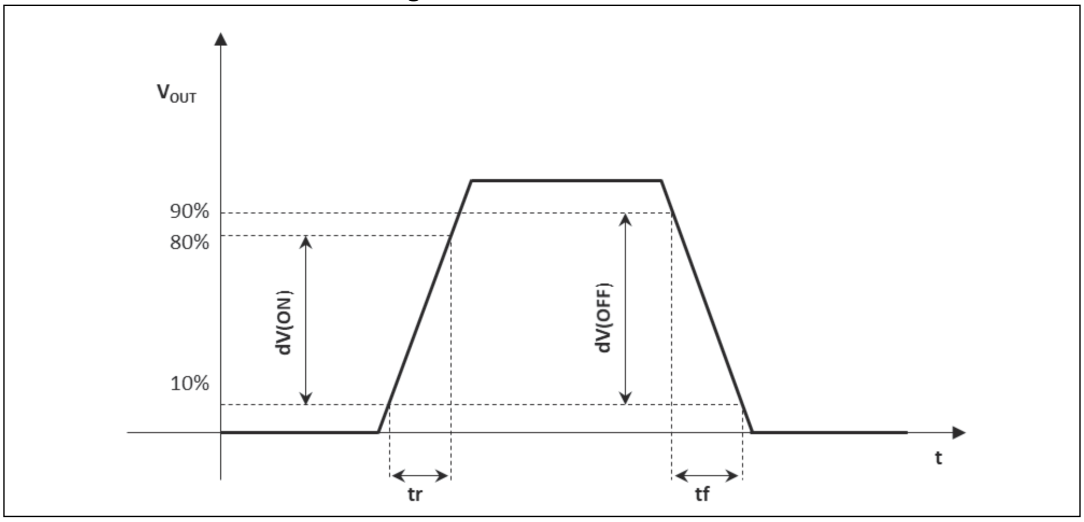


Figure 5. td(ON)-td(OFF) definition

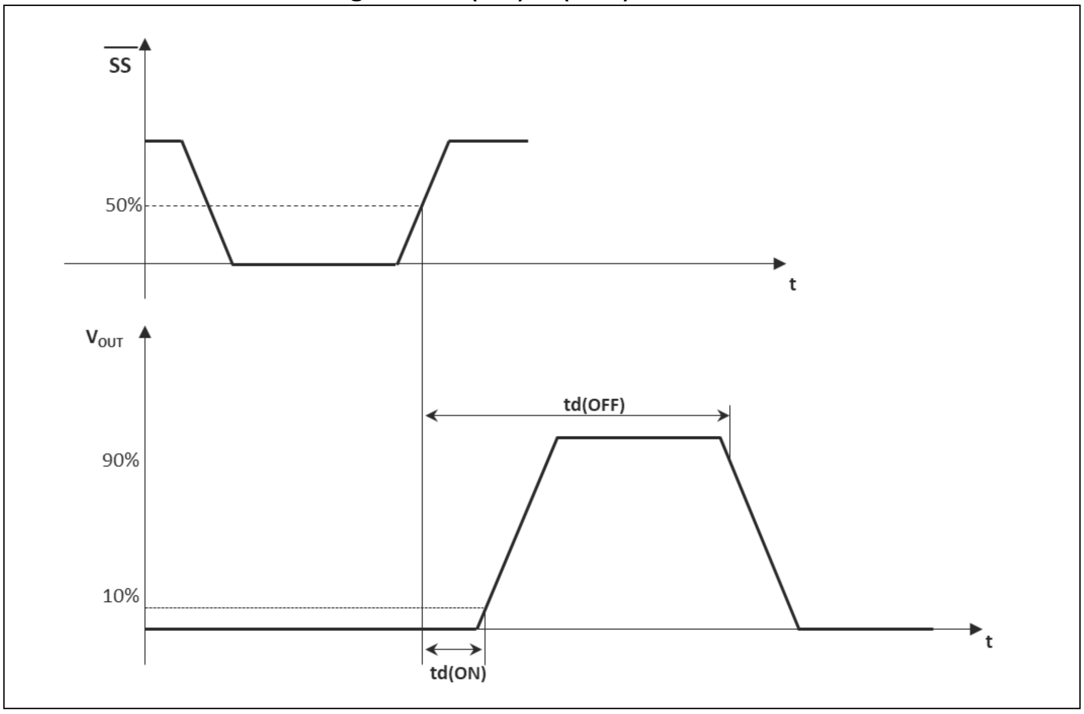


Table 8. Logic inputs and output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	$\overline{SS}$, CLK, SDI and OUT_EN low level voltage		-0.3		0.3 x V_{DD}	V
V_{IH}	$\overline{SS}$, CLK, SDI and OUT_EN high level voltage		0.7 x V_{DD}		V_{DD} +0.3	V
$V_{I(HYST)}$	$\overline{SS}$, CLK, SDI and OUT_EN hysteresis	V_{DD} = 5 V		100		mV
I_{IN}	$\overline{SS}$, CLK, SDI and OUT_EN current	V_{IN} = 5 V	10			µA
V_{SDOH}	SDO high level voltage	I_{SDO} = -1 mA	V_{DD}-0.2			V
V_{SDOL}	SDO low level voltage	I_{SDO} = +2 mA			0.2	V

Table 9. Serial interface timings (V_{DD} = 5 V; V_{CC} = 24 V; -40°C < T_J < 125°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
fCLK	SPI clock frequency				20	MHz
T_{CLK}	SPI clock period		50			ns
tr(CLK) tf(CLK)	SPI clock rise/fall time (see *Figure 7*, *8*)				5	ns
tsu(SS)	SS setup time (see *Figure 7*, *8*)		80			ns
th(SS)	SS hold time (see *Figure 7*, *8*)		80			ns
tc(SS)	SS disable time (see *Figure 7*, *8*)		20			µs
tw(CLK)	CLK high time (see *Figure 7*, *8*)		15			ns
tsu(SDI)	Data input setup time (see *Figure 7*, *8*)		6			ns
th(SDI)	Data input hold time (see *Figure 7*, *8*)		6			ns
ta(SDO)	Data output access time (see *Figure 7*, *8*)	$R_{PULL-DOWN}$ = 300 Ω C_{LOAD} = 50 pF			25	ns
tdis(SDO)	Data output disable time (see *Figure 7*, *8*)				20	ns
tv(SDO)	Data output valid time (see *Figure 7*, *8*)				20	ns
t_{JITTER}	Jitter on single channel $t_{CYCLE(SS)}$ = 20 µs				6	µs
	Jitter on single channel $t_{CYCLE(SS)}$ < 20 µs				20	

Table 10. Internal communication timings (V_{DD} = 5 V; V_{CC} = 24 V; -40°C < T_J < 125°C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$f_{refresh}$	Refresh delay			15		kHz
t_{WD}	Watchdog time		272	320	400	µs

Table 11. Insulation and safety-related specifications

Symbol	Parameter	Test conditions	Value	Unit
CLR	Clearance (minimum external air gap)	Measured from input terminals to output terminals, shortest distance through air	3.3	mm
CPG	Creepage (minimum external tracking)	Measured from input terminals to output terminals, shortest distance path along body	3.3	mm
CTI	Comparative tracking index (tracking resistance)	DIN IEC 112/VDE 0303 part 1	≥600	V
	Isolation group	Material group (DIN VDE 0110, 1/89, Table 1)	I	-

Table 12. Insulation characteristics

Symbol	Parameter	Test condition	Value	Unit
IEC 60747-5-5				
V_{IORM}	Maximum working isolation	-	937	V_{PEAK}
V_{PR}	Input-to-output test voltage	Method a, type test, V_{PR} = V_{IORM} x 1.6, tm = 10s partial discharge < 5 pC	1500	V_{PEAK}
		Method b, 100% production test, V_{PR} = V_{IORM} x 1.875, tm = 1s partial discharge < 5 pC	1758	V_{PEAK}
V_{IOTM}	Transient overvoltage	Type test; t_{ini} = 60 s	4245	V_{PEAK}
V_{IOSM}	Maximum surge insulation voltage	Type test	4245	V_{PEAK}
R_{IO}	Insulation resistance	V_{IO} = 500 V at ts	$>10^9$	Ω
UL1577				
V_{ISO}	Insulation withstand voltage	1 min. type test	2500/3536	V_{rms}/V_{PEAK}
V_{ISO} test	Insulation withstand test	1 sec. 100% production	3000/4245	V_{rms}/V_{PEAK}

6 Serial interface

6.1 Functional description

An integrated SPI peripheral permits to have a fast communication interface between external microcontroller and IC purposing, both to drive the Power Stage outputs and check the per-channel OVT diagnostic information of the device. Daisy chaining is allowed.

It follows the timing requirement established by the synchronous serial communication standard and works up to 20 MHz communication speed.

The communication implemented expects 8-bit data communication; the frame sent by the microcontroller contains only the status of the channels (ON or OFF), while the frame received by the microcontroller contains the information regarding channel fault condition (bit “0” related to a channel running represents normal operation, whereas a bit 1 represents a fault condition).

SDI frame

MSB							LSB
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

SDO frame

MSB							LSB
F7	F6	F5	F4	F3	F2	F1	F0

6.2 Serial data in (SDI)

This pin is the IC input of the serial command frame (MOSI). SDI is reading on CLK rising edges and, thus, the microcontroller must change SDI state during the CLK falling edges.

SDI pin is tri-stated when one of the following conditions is met:

- $\overline{\text{SS}}$ signal is high.
- OUT_EN pin is active.

The bits sent through the SDI line are shifted in the internal Output Status Register. In daisy chaining communication the microcontroller maintains the $\overline{\text{SS}}$ low after the 8th bit to allow the shift of the Output Status Register to the SDO line. The bits in the Output Status Register are frozen by the internal logic when the $\overline{\text{SS}}$ goes high.

6.3 Serial data out (SDO)

This pin is the IC output of the serial fault frame (MISO). The information on SDO is updated on CLK falling edges; the microcontroller reads SDO frame on CLK rising edges as established by standard. At communication startup, when $\overline{\text{SS}}$ falling edge is coming, just the first bit of the frame is available.

SDO pin is tri-stated when $\overline{\text{SS}}$ signal is high.

In daisy chaining communication and OUT_EN driven high, the SDO line transfers the content of the internal Output Status Register after the 8th CLK pulse.

6.4 Serial data clock (CLK)

The CLK line is the IC input clock for serial data sampling. SDO is updated on CLK falling edges, and then it must be sampled on the rising edge. The SDI line is sampled on SCK rising edges.

When the SS signal is high (slave not selected), the microcontroller should drive the CLK low (settings for MCU SPI port are CPHA = 0 and CPOL = 0).

6.5 Slave select ($\overline{SS}$)

Slave select $\overline{SS}$ signal is used to enable the ISO8200AQ serial communication shift register. Data is flushed in through the SDI pin and out from the SDO pin only when the $\overline{SS}$ pin is low. On the $\overline{SS}$ pin falling edge the Fault Register (containing IC fault conditions) is frozen, so any changing on the channel status is latched until the next $\overline{SS}$ falling edge event, the SDO is enabled and at the same time the internal refresh is disabled too. On the $\overline{SS}$ pin rising edge event the 8 bits in the Output Status Register are frozen and the outputs of the Process Stage are driven accordingly. If more than 8 bits are flushed into the IC, only the last 8 are evaluated, the other ones are flushed out from the SDO pin after fault condition bits; this way a proper communication is granted also in a daisy chain configuration.

Figure 6. SPI mode diagram

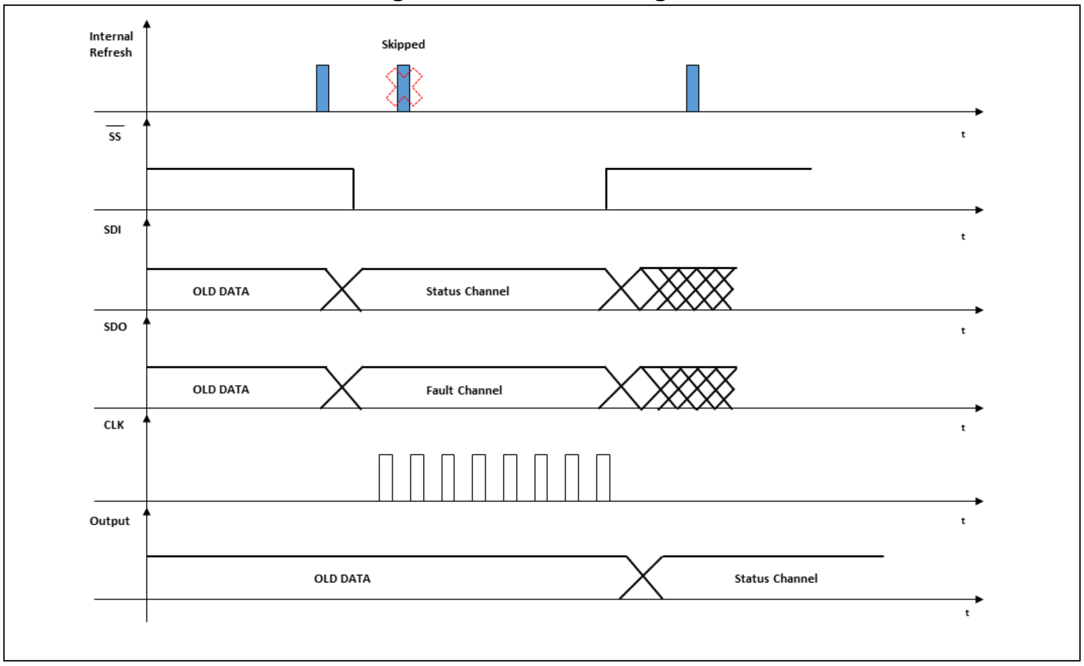


Figure 7. SPI input timing diagram

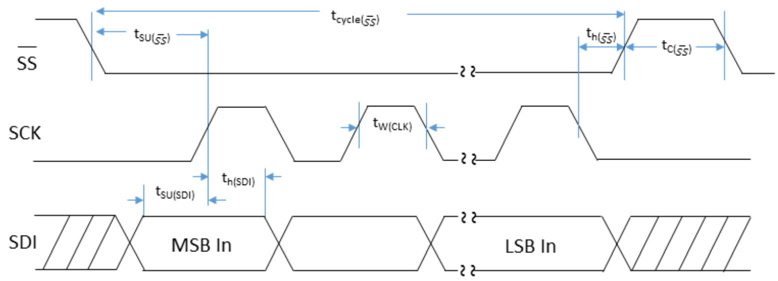
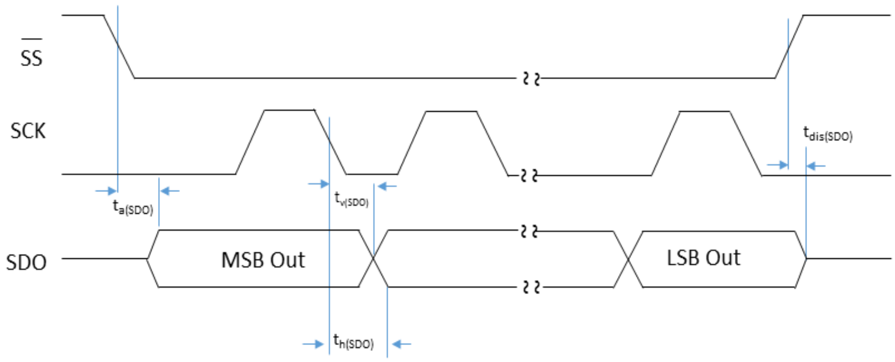


Figure 8. SPI output timing diagram



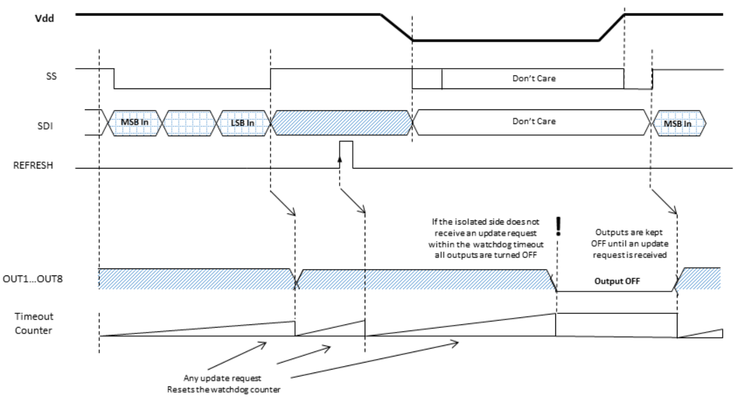
6.5.1 Watchdog

The IC is composed of two chips (Logic Stage and Process Stage) supplied by two independent and galvanic isolated sources (V_{DD}/GND_{DD} and V_{CC}/GND_{CC} pins, respectively).

The IC provides a watchdog function in order to guarantee a safe condition of the Process Stage when V_{DD} (or GND_{DD}) supply voltage is missing. At the end of each SPI communication the channel status register is transferred to the Process Stage that both resets an internal timeout counter and turns ON/OFF the outputs accordingly. If the Logic Stage does not update the output status within tWD, all the outputs of the Process Stage are disabled until a new update request is received (this also happens if $\overline{SS}$ stays low for a time longer than t_{WD}).

Independently of the SPI communication, the Logic Stage chip periodically sends a refresh signal to the Process Stage chip. The refresh signal is also considered a valid update signal to reset the timeout counter on the Process Stage, so the isolated side watchdog does not protect the system from a failure of the host controller (e.g. MCU freezing).

Figure 9. Watchdog behavior



6.5.2 Output enable (OUT_EN)

This pin provides a fast way to disable all the outputs simultaneously. When the *OUT_EN* pin is driven low for at least tw (OUT_EN), all eight outputs are disabled. This timing execution is compatible with an external reset push from the operator and/or safety requirements.

Note that the OUT_EN signal acts as a reset for the internal data register driving the output switches: when the OUT_EN is low, SDO is pulled down and the output stage is forced OFF. To re-enable SDO it is necessary to raise the *OUT_EN* pin; to enable back the output stage it is then necessary to raise the *OUT_EN* pin and send the desired output configuration by an SPI command.

Figure 10. OUT_EN without effect on output

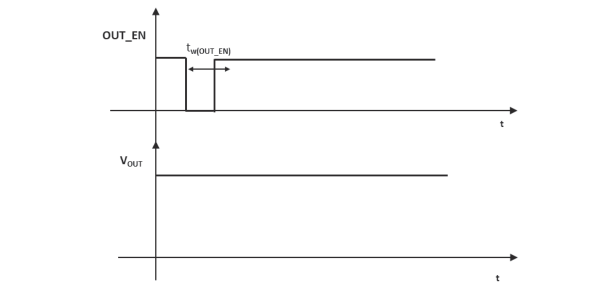
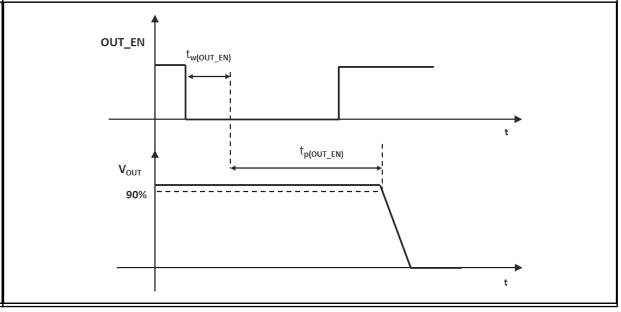


Figure 11. OUT_EN effective on output channel



6.6 FAULT and PGOOD indications

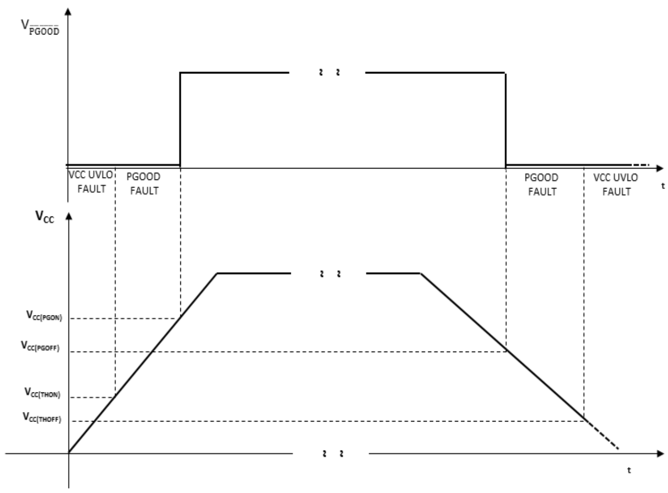
The $\overline{\text{FAULT}}$ pin is an active low open drain output indicating fault conditions. This pin is activated when at least one of the following conditions occurs:

- Junction overtemperature (TJX >TJSD) of one or more channels of the Process Stage. The MISO signal can be used to detect which channels are in thermal fault (per-channel OVT diagnostic);
- No module-8 SPI communication (the number of bits sent through the SDI is not a multiple of 8);
- Internal communication error. In fact, the IC is able to identify (and report to the microcontroller) if any error in the data transmission between isolation happened. When it should happen, the output stage maintains the previous ON/OFF status.

The $\overline{\textit{PGOOD}}$ pin is an active low open drain output indicating if the supply voltage of the Process Stage chip is lower than the internal threshold (see *Figure 12*).

Note: When $\overline{\textit{SS}}$ signal is low the transmission between Control Logic Stage and Process Stage is inhibited and the status of $\overline{\textit{PGOOD}}$ is not refreshed ($\overline{\textit{PGOOD}}$ refresh time < 120 us).

Figure 12. Power GOOD pin behavior



6.7 Truth table

Table 13. Truth table

Condition	Status register BIT_x	OUT_x	Fault register BIT_x	$\overline{FAULT}$	$\overline{PGOOD}$
Normal operation	1	ON	0	H (not active)	H (not active)
	0	OFF	0		
Thermal Junction (T_{JX}> T_{JSD})	1	OFF	1	L (active)	Don‘t care
	0	OFF	1	H (not active)	
Thermal Case T_C > T_{CSD}	See *Figure 20*			Don‘t care	Don‘t care
V_{CC} UVLO FAULT (*Figure 12*)	0	OFF	X	X	L (active)
	1				
POWER GOOD FAULT (*Figure 12*)	1	ON	Don‘t care	Don‘t care	L (active)
	0	OFF			
V_{DD} UVLO (Watchdog)	X	OFF	X	H (not active)	H (not active)
SPI FAULT (module-8 violation)	X	X	Don‘t care	L (active)	Don‘t care
Internal communication error	X	X	X	L (active)	Don‘t care

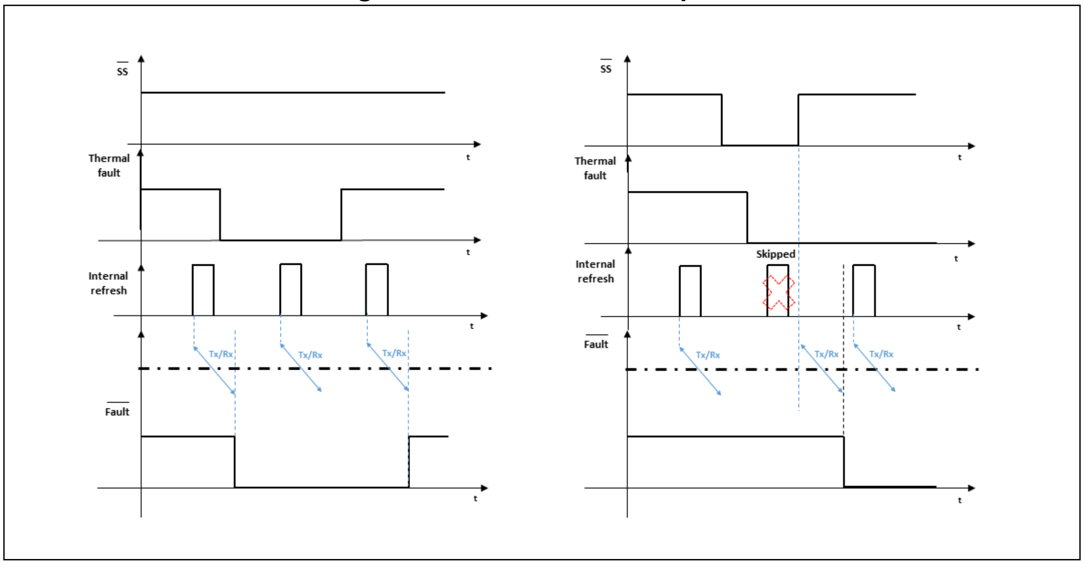
x: maintain the previous condition.

6.7.1 Junction overtemperature

The thermal status of the device is updated during each transmission sequence between the two isolated stages.

When $\overline{SS}$ is low the communication between the two stages is disabled. In this case the thermal status of the device cannot be updated and the $\overline{FAULT}$ indication may be different to the actual status. In any case the thermal protections of the channel outputs in the Process Stage are always operative.

Figure 13. Thermal status update



7 Power section

7.1 Current limitation

The current limitation process is activated when the current sense connected on the output stage measures a current value higher than a fixed threshold. When this condition is verified the gate voltage is modulated to avoid output current increasing over the limitation value. The following figures (where BIT_X is intended as X^{TH} bit of the Output Status Register) show typical output current waveforms with different load conditions.

Figure 14. Switching on resistive load

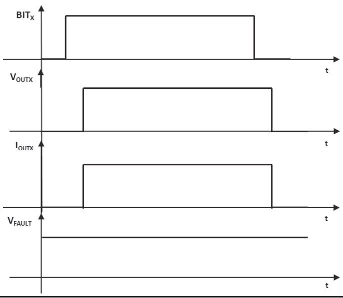


Figure 15. Switching on bulb lamp

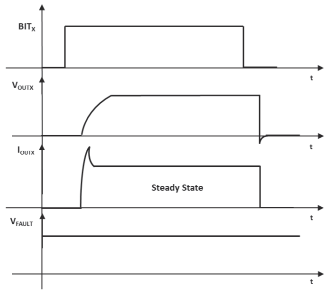


Figure 16. Switching on light inductive load

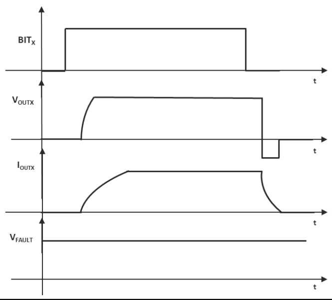


Figure 17. Switching on heavy inductive load

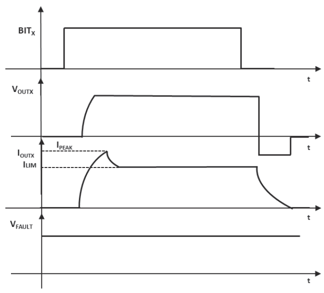


Figure 18. Short-circuit during ON state

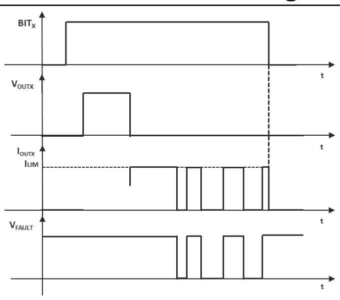
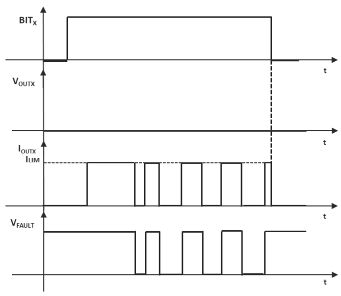


Figure 19. Switching on short-circuit



7.2 Thermal protection

The device is protected against overheating due to overload conditions. During driving period, if the output is overloaded, the device suffers two different thermal stresses, the first one related to the junction, and the second related to the case.

The two faults have different trigger thresholds: the junction protection threshold (T_{JSD}) is higher than that of the case protection (T_{CSD}); generally the first protection that is activated in thermal stress conditions is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it goes below the reset threshold (T_{JR}). This behavior continues until the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated and the output is switched off and back on when the junction temperature of each channel in fault and case temperature are below the respective reset thresholds.

Figure 20. Thermal protection flowchart

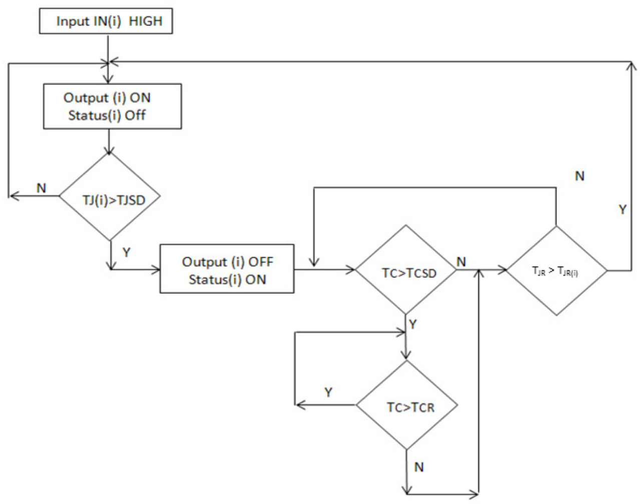


Figure 21. Thermal protection and fault behavior (T_{JSD} triggered before T_{CSD})

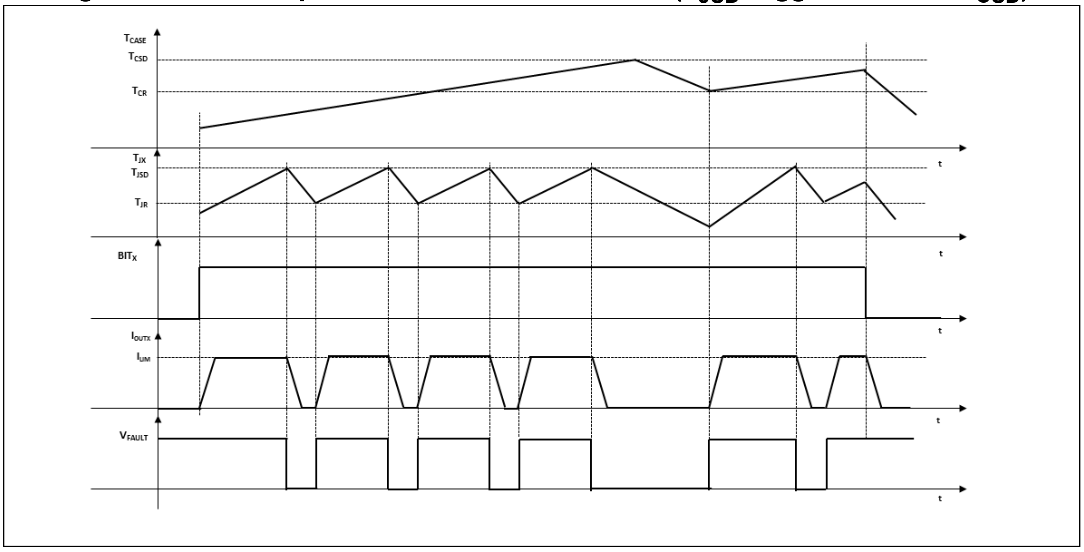
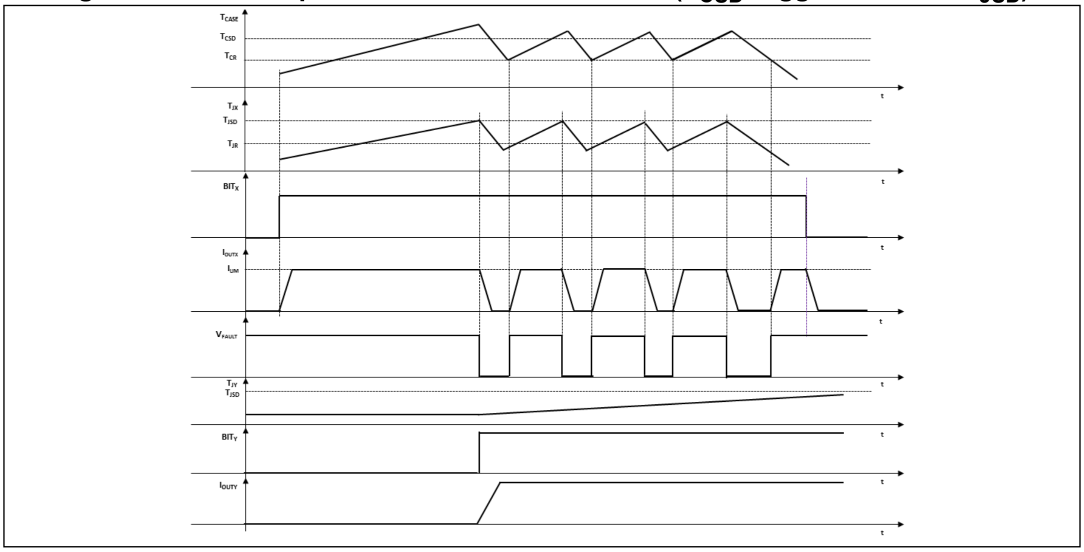


Figure 22. Thermal protection and fault behavior (T_{CSD} triggered before T_{JSD})



8 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions:

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode in parallel to a resistor between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

Equation 1

$$R_{GND} \geq V_{CC}/I_{GNDcc}$$

where I_{GNDcc} is the DC reverse ground pin current and can be found in *Section 3: Absolute maximum ratings on page 9* of this datasheet.

Power dissipated by R_{GND} during reverse polarity situation is:

Equation 2

$$P_D = (V_{CC})^2/R_{GND}$$

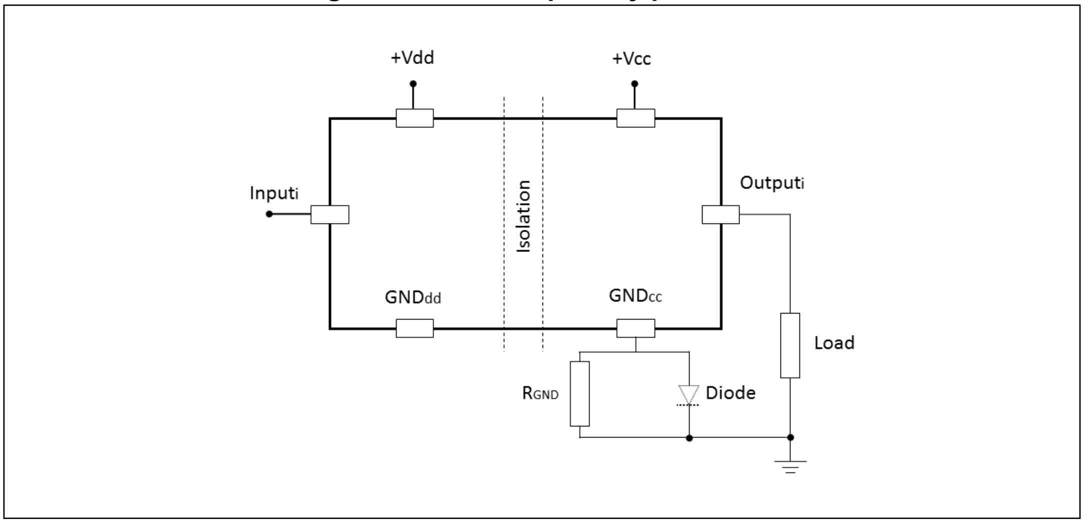
If option 2 is selected, the diode has to be chosen by taking into account VRRM > $|V_{CC}|$ and its power dissipation capability:

Equation 3

$$P_D \geq I_S * V_F$$

*Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the system. Using option 1, ΔV = Rgnd * Icc. Using option 2, ΔV = VF@(IF).*

Figure 23. Reverse polarity protection



Note: Input(i) is intended as any input pin on logic side.

This schematic can be used with any type of load.

9 Reverse polarity on V_{DD}

The reverse polarity on V_{DD} can be implemented on board by placing a diode between the GND_{DD} pin and GND digital ground.

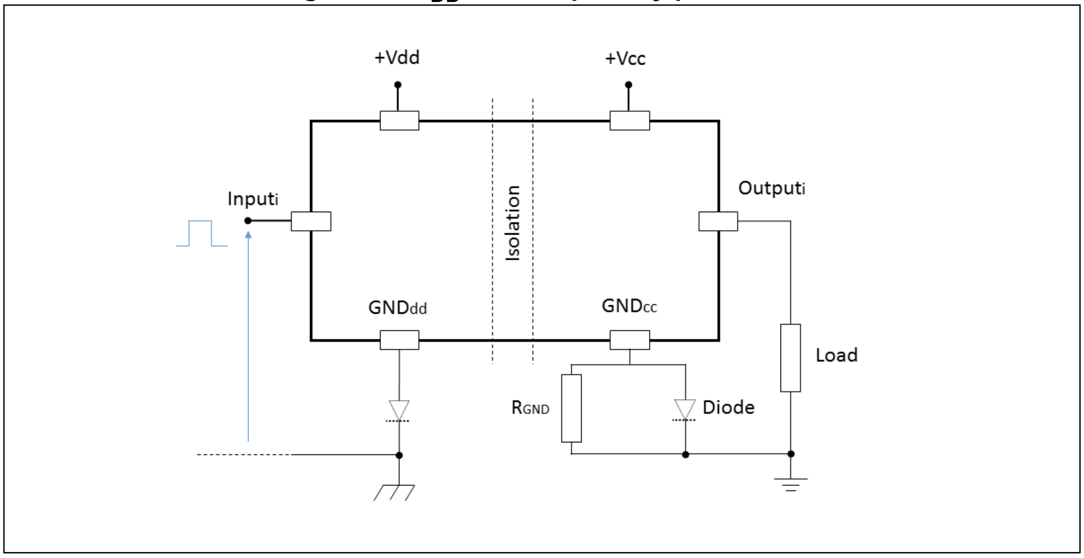
The diode has to be chosen by taking into account VRRM >|V_{DD}| and its power dissipation capability:

Equation 4

$$P_D \geq I_{DD} * V_F$$

Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV = VF@(Idd)) between GND_{DD} of the device and digital ground of the system. In order to guarantee to proper triggering of the input signal, ΔV(max.) must result lower than $V_{IH(MIN)}$.

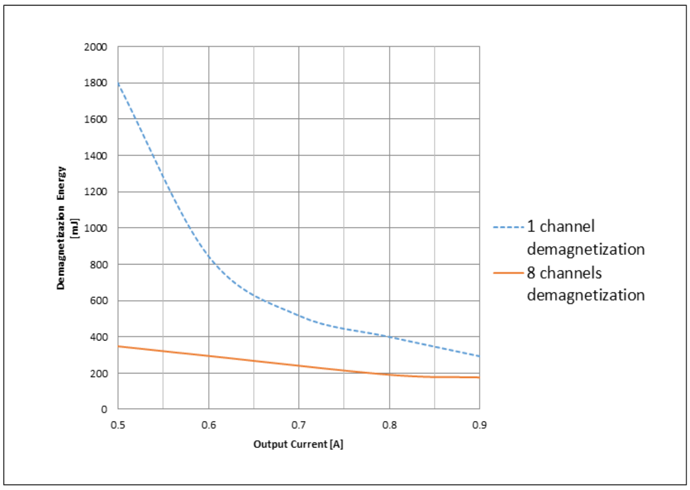
Figure 24. V_{DD} reverse polarity protection



Note: Input(i) is intended as any input pin on logic side.

10 Demagnetization energy

Figure 25. Single pulse demagnetization energy vs. load current (Typical values at TAMB = 125°C)

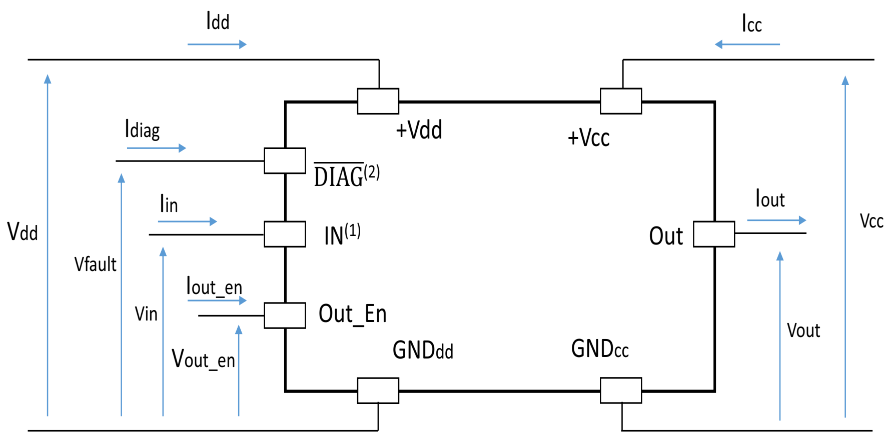


11 Conventions

11.1 Supply voltage and power output conventions

Figure 26 shows all conventions used in this document for voltage and current usage.

Figure 26. Supply voltage and power output conventions

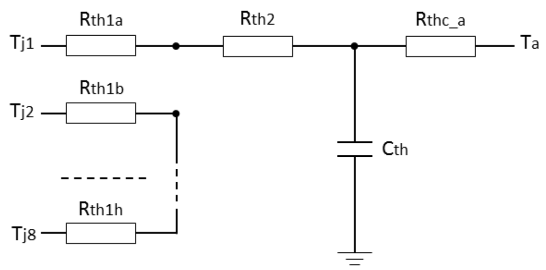


(1): intended as any input pin on logic side
(2): intended as any open drain pin on logic side

12 Thermal information

12.1 Thermal impedance

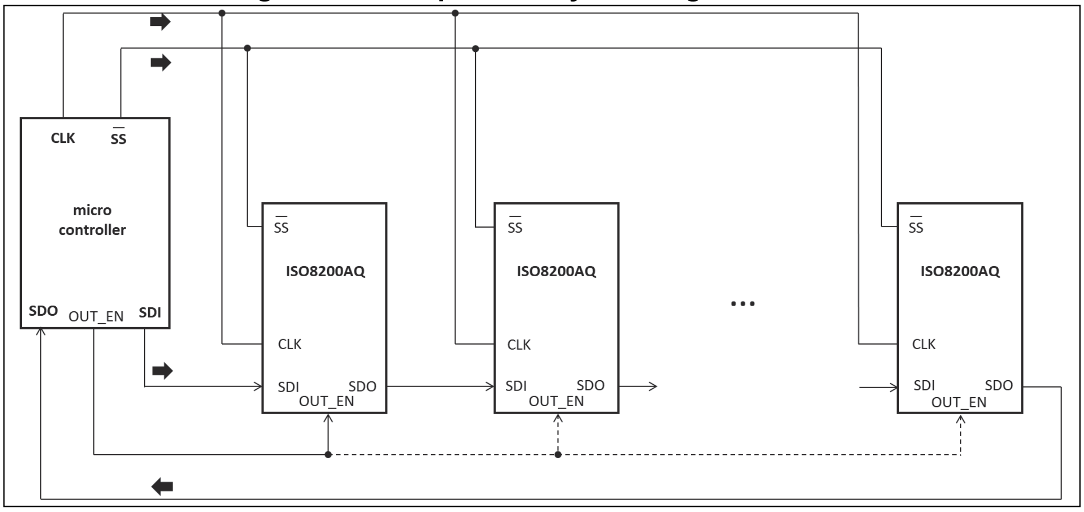
Figure 27. Simplified thermal model of the process stage



13 Daisy chaining

ISO8200AQ can be daisy chained by connecting the serial data output (SDO) of one device to the digital input (SDI) of the following device in the chain (see *Figure 28*).

Figure 28. Example of daisy chaining connection



14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

14.1 TFQFPN32 package information

Figure 29. TFQFPN32 outline

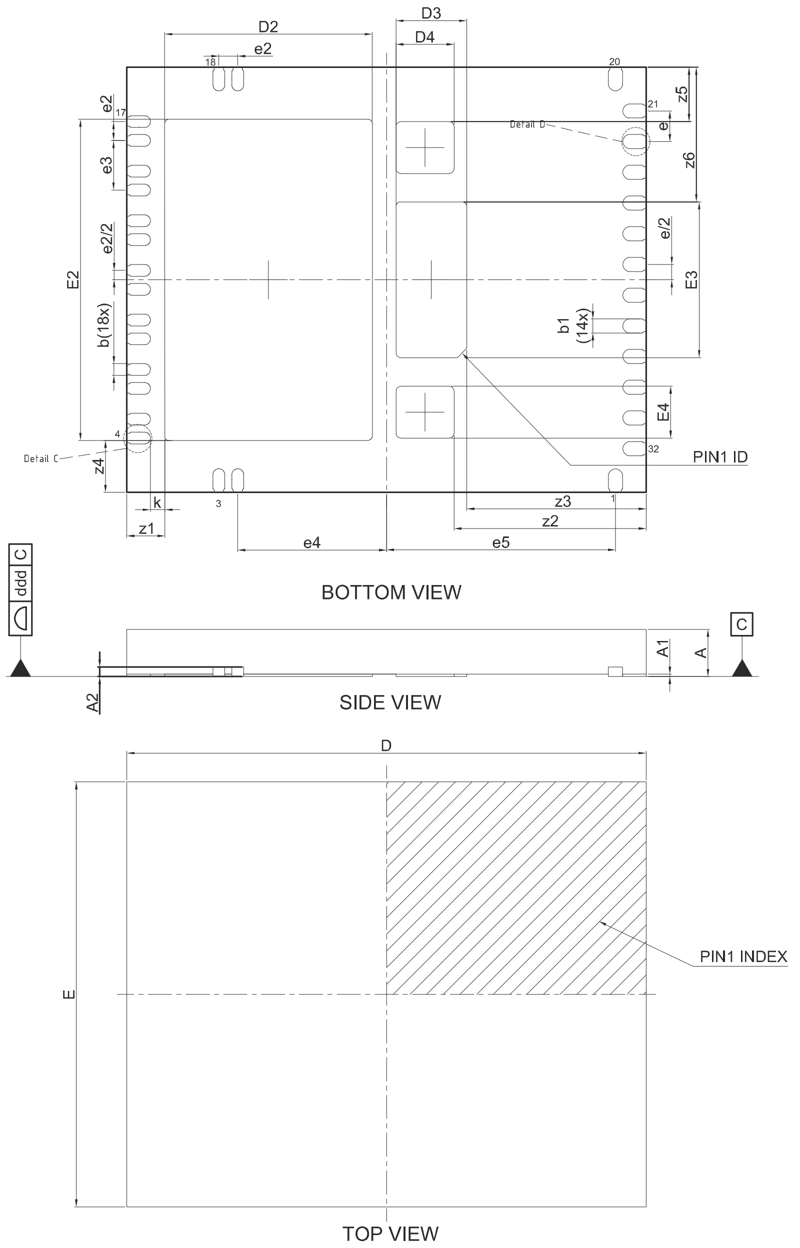


Figure 30. Package details

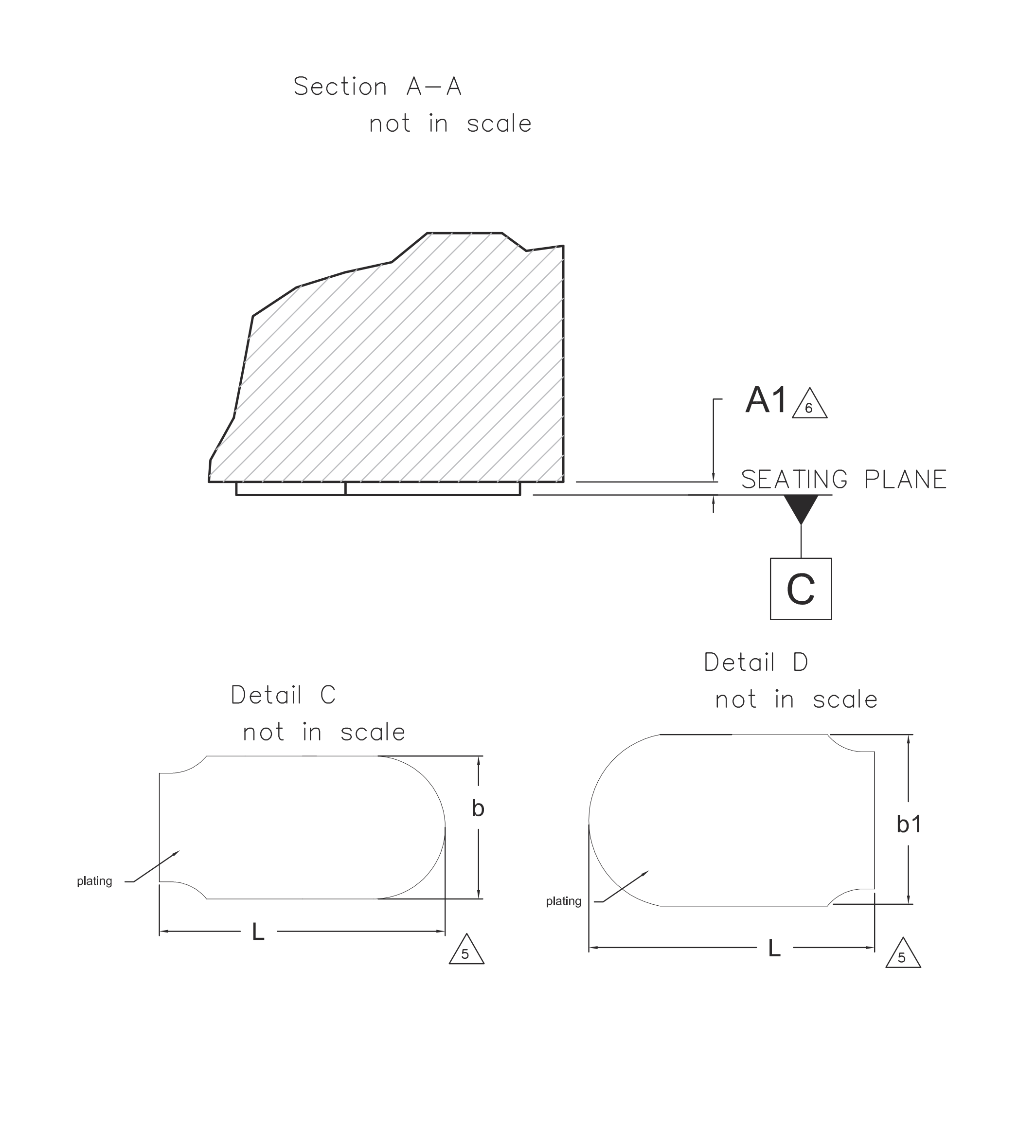


Table 14. TFQFPN32 mechanical data

Dim	mm		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
A1	0		0.05
A2		0.20 REF	
b(1)	0.20	0.25	0.30
b1(1)	0.25	0.30	0.35
D	10.90	11.0	11.10

Table 14. TFQFPN32 mechanical data (continued)

Dim	mm		
	Min.	Typ.	Max.
E(1)	8.90	9.00	9.10
D2	4.30	4.40	4.50
E2	6.70	6.80	6.90
D3	1.40	1.50	1.60
E3	3.20	3.30	3.40
D4	1.13	1.23	1.33
E4	1.00	1.10	1.20
e		0.65	
e2		0.40	
e3		1.05	
e4		3.15	
e5		4.85	
k	0	0.30	
z1		0.80	
z2		4.07	
z3		3.80	
z4		1.10	
z5		1.15	
z6		2.85	
L(1)	0.45	0.50	0.55

1. Dimensions “b” and “L” are measured at terminal plating surface.

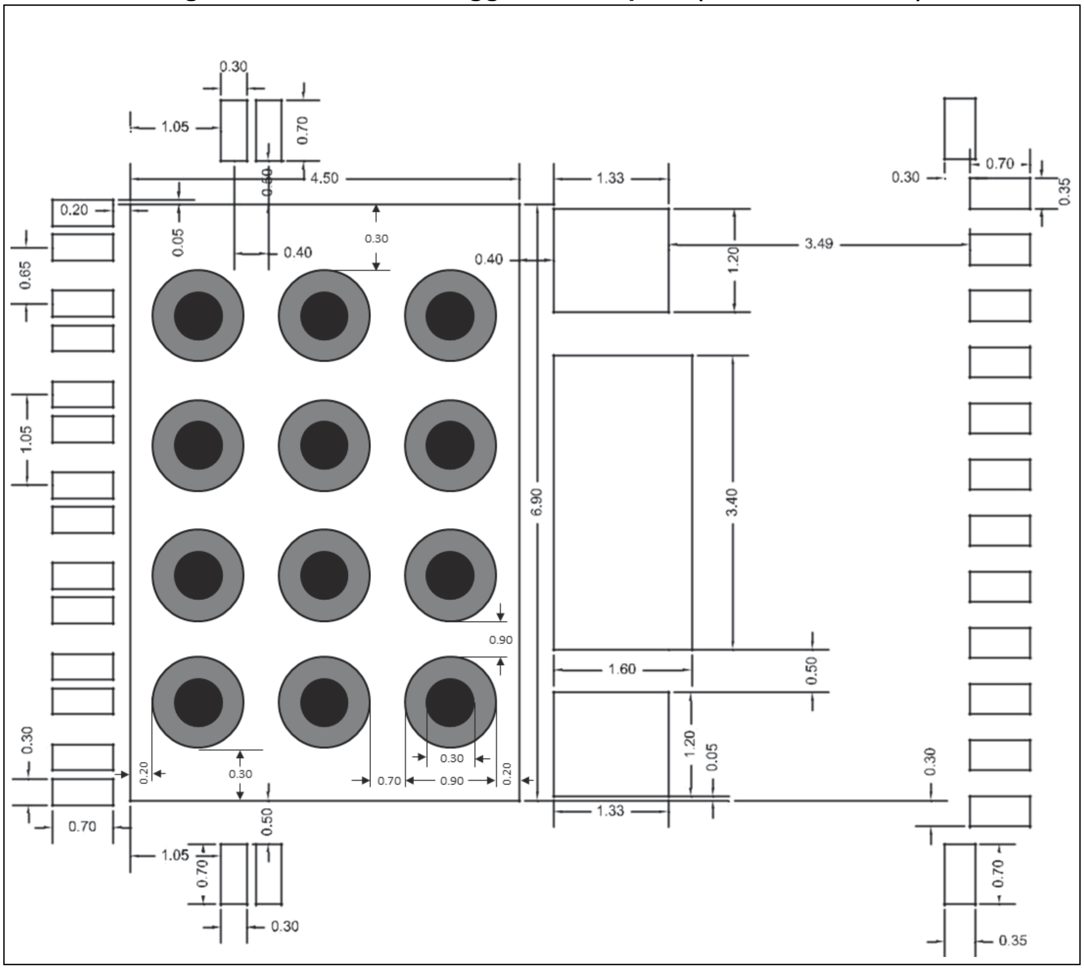
Table 15. Rev 4

Symbol	Tolerance of form and position	Definition	Notes
aaa	0.15	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
bbb	0.10	The tolerance that controls the position of the entire terminal pattern with respect to datum's A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to datum's A and B.	
ccc	0.10	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	

Table 15. Rev 4 (continued)

Symbol	Tolerance of form and position	Definition	Notes
ddd	0.08	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".	This tolerance is normally compounded with tolerance zone defined by bbb.
eee	0.08	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the "coplanarity" of the package terminals.
fff	0.10	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone will be datum's defined by the centerlines of the package body.	
REF	-	-	No tolerance for A2

Figure 31. TFQFPN32 suggested footprint (measured in mm)



15 Packing information

15.1 TFQFPN32 packing information

15.1.1 TFQFPN32 packing method concept

Figure 32. TFQFPN32 packing method concept

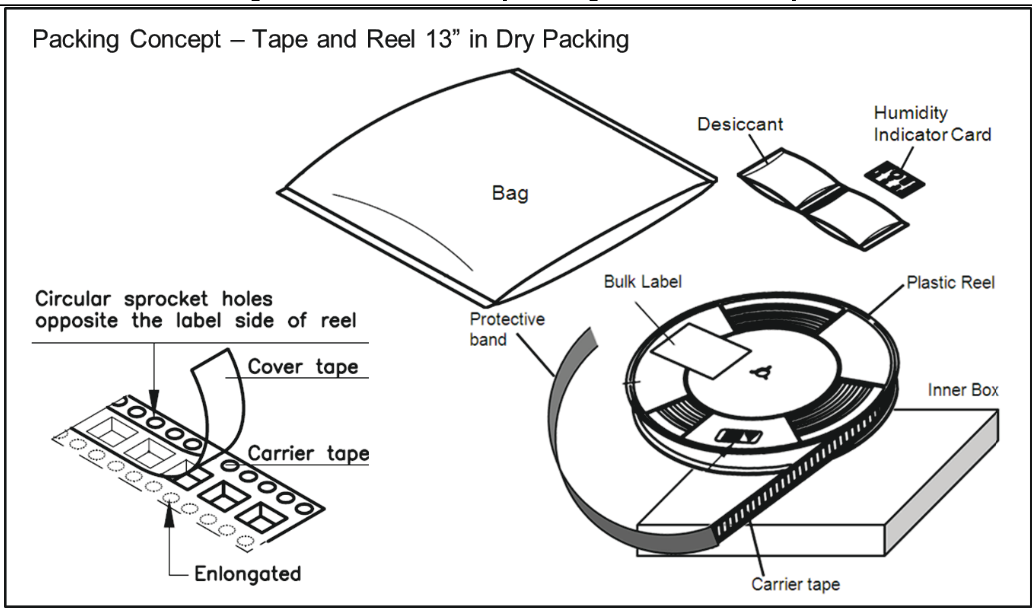
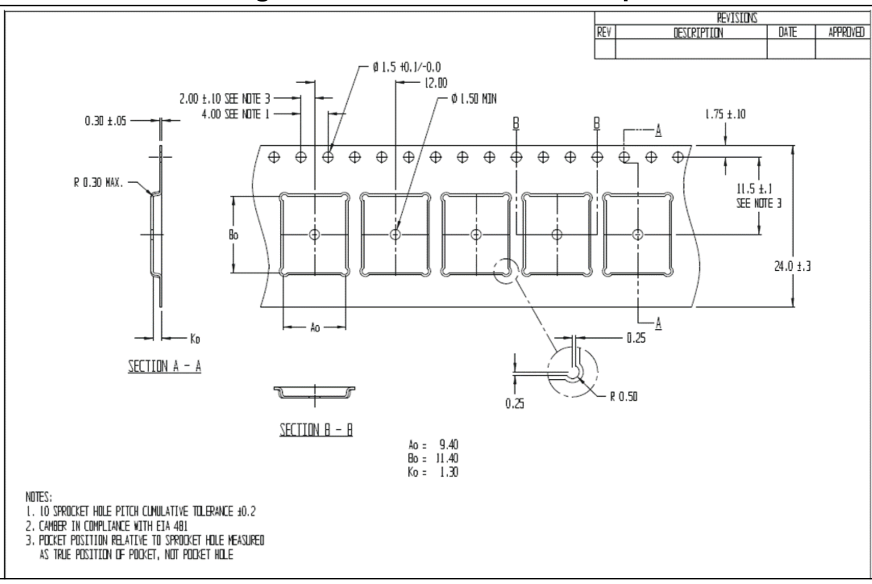
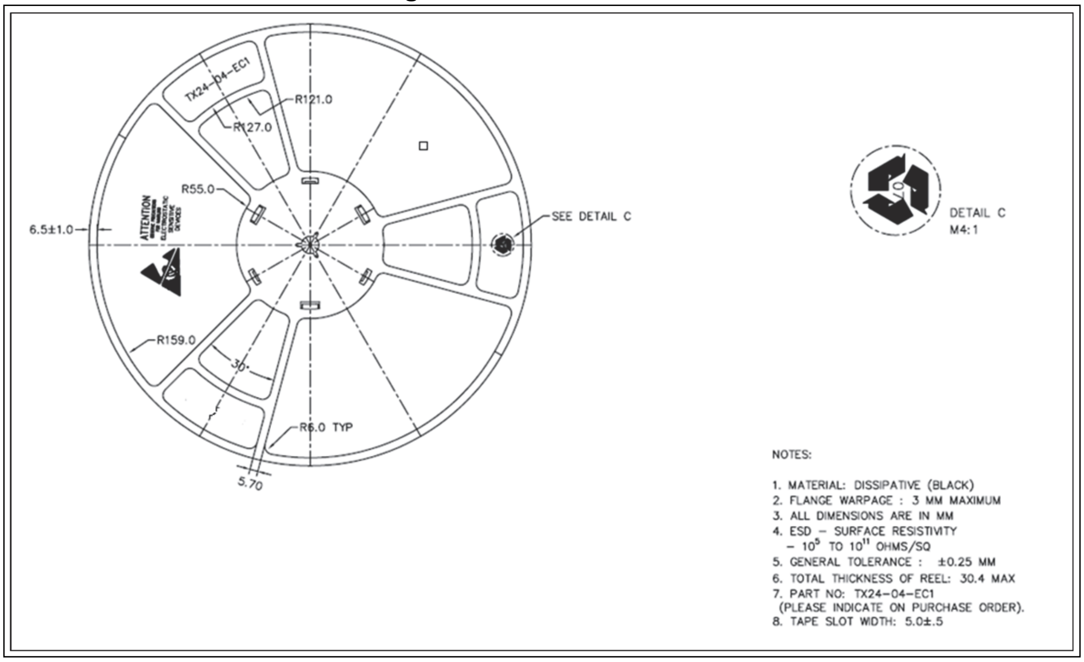


Figure 33. TFQFPN32 carrier tape



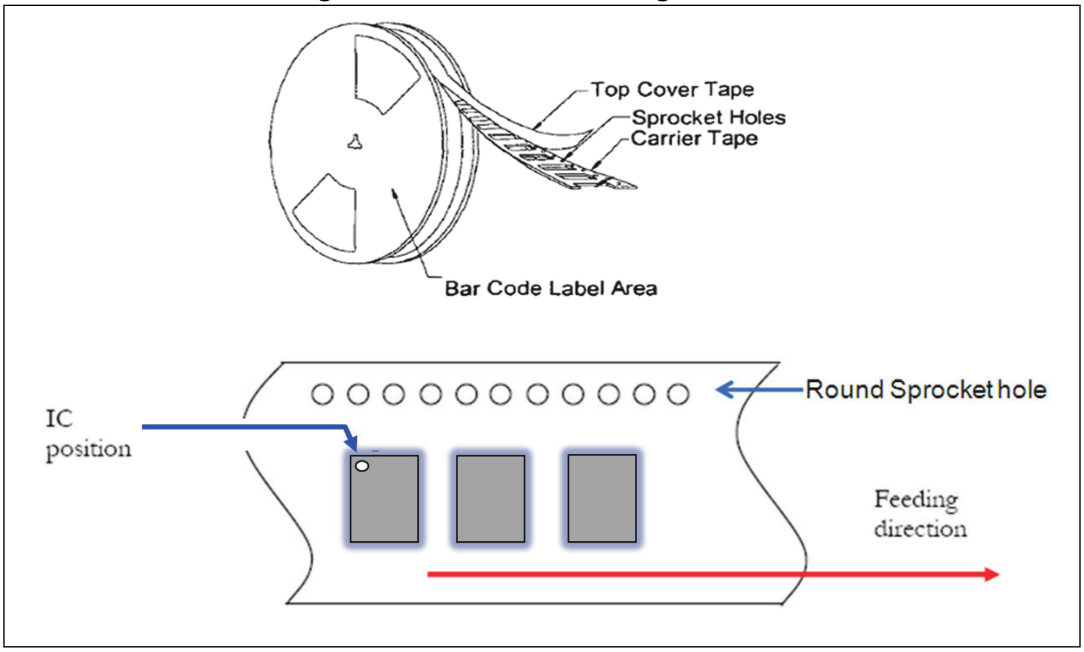
Reel – 330 mm diameter x 101 mm hub x 24 mm width.

Figure 34. TFQFPN32 reel



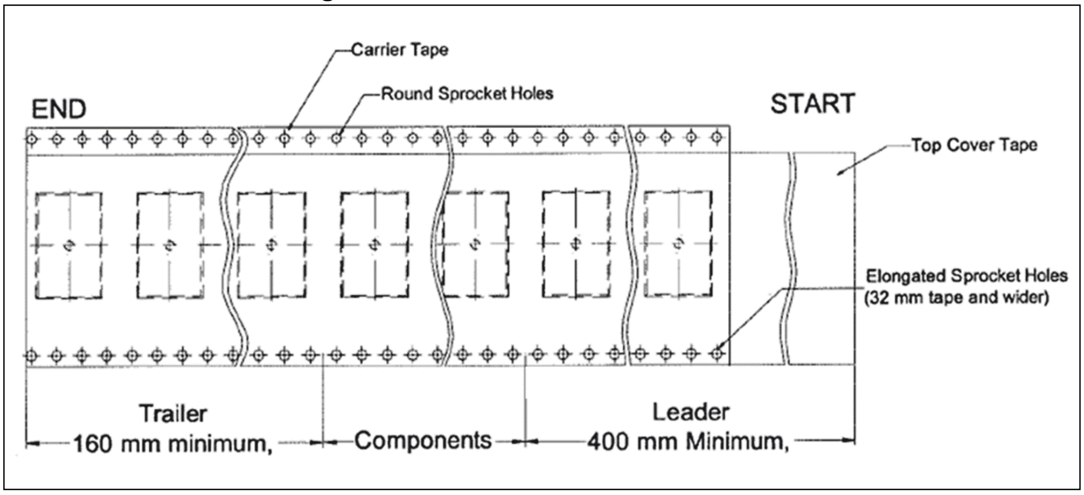
15.1.2 TFQFPN32 winding direction

Figure 35. TFQFPN32 winding direction



15.1.3 TFQFPN32 leader and trailer

Figure 36. TFQFPN32 leader and trailer



Note: Leader and trailer length as per EAI-481specification.

16 Ordering information

Table 16. Ordering information

Part number	Package	Packaging
ISO8200AQ	TFQFPN32	Tube
ISO8200AQTR	TFQFPN32	Tape and reel

17 Revision history

Table 17. Document revision history

Date	Revision	Changes
31-Oct-2018	1	Initial release.
3-Dec-2018	2	Updated *Figure 1* and *Figure 28*, amended *Table 8*
2-Jun-2019	3	Features updated. *Table 1* & *Table 2* modified. *Figure* replaced. Small changes to the text.
23-Apr-2020	4	*Table 12* and *14* updated. *Figure 29* replaced and *Table 15* added.