SECONDARY SIDE SYNCHRONOUS RECTIFICATION SWITCHER

Description

The APR34910 is a secondary-side combo IC combining an N-channel MOSFET and a driver circuit designed for synchronous rectification (SR).

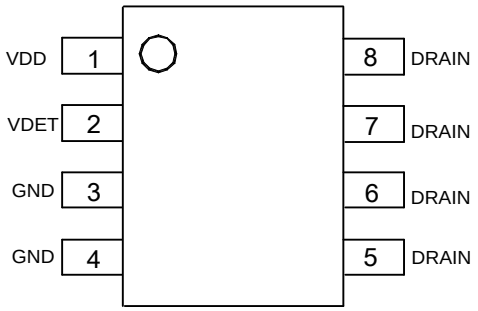
The APR34910 supports continuous and discontinuous conduction mode (CCM and DCM) and quasi-resonant flyback operation. It not only provides a short turn-on and turn-off delay to reduce power loss, but also eliminates false trigger to keep safe operation without adding any external components or circuitry.

The APR34910 can be charged by internal PLR (Pulse Linear Regulator) at low system output voltage and can provide a wide output operation voltage from 3.3V to 24V.

The APR34910 is available in the SO-8 (Type CJ2) package.

Pin Assignments

(Top View)



SO-8 (Type CJ2)

Features

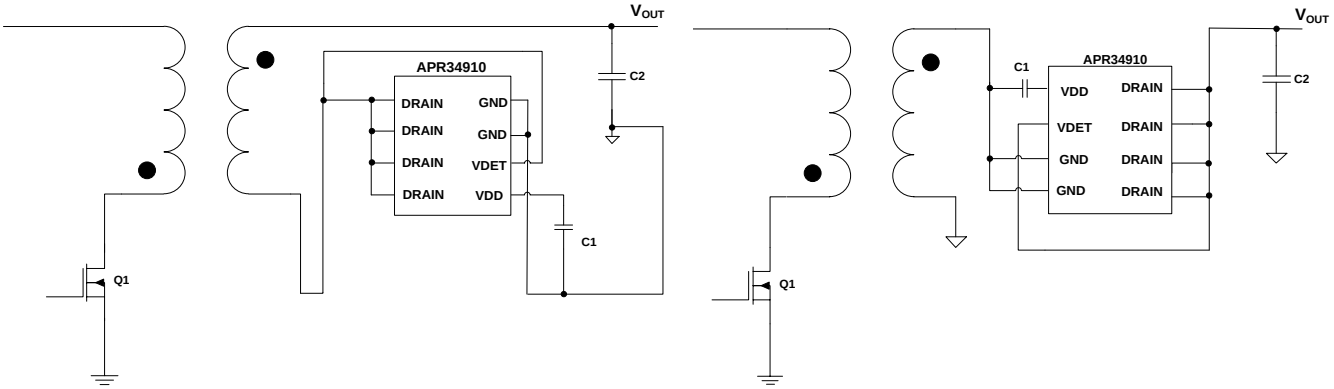
- Supports Flyback Synchronous Rectification with CCM/DCM/QR Operation Mode
- Intelligent Control to Minimize Turn-On and Turn-Off Delay
- Smart-Blanking Control to Prevent Shoot Through
- Support Both High-Side and Low-Side Application
- Built-in PLR Power Supply for Low System Output Voltage
- Internal UVLO Protection
- Fewest External Components
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Smart phone quick chargers
- Notebook computer adaptors
- Set-top box (STB) power supplies
- Other compact switching AC-DC adaptors/chargers

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



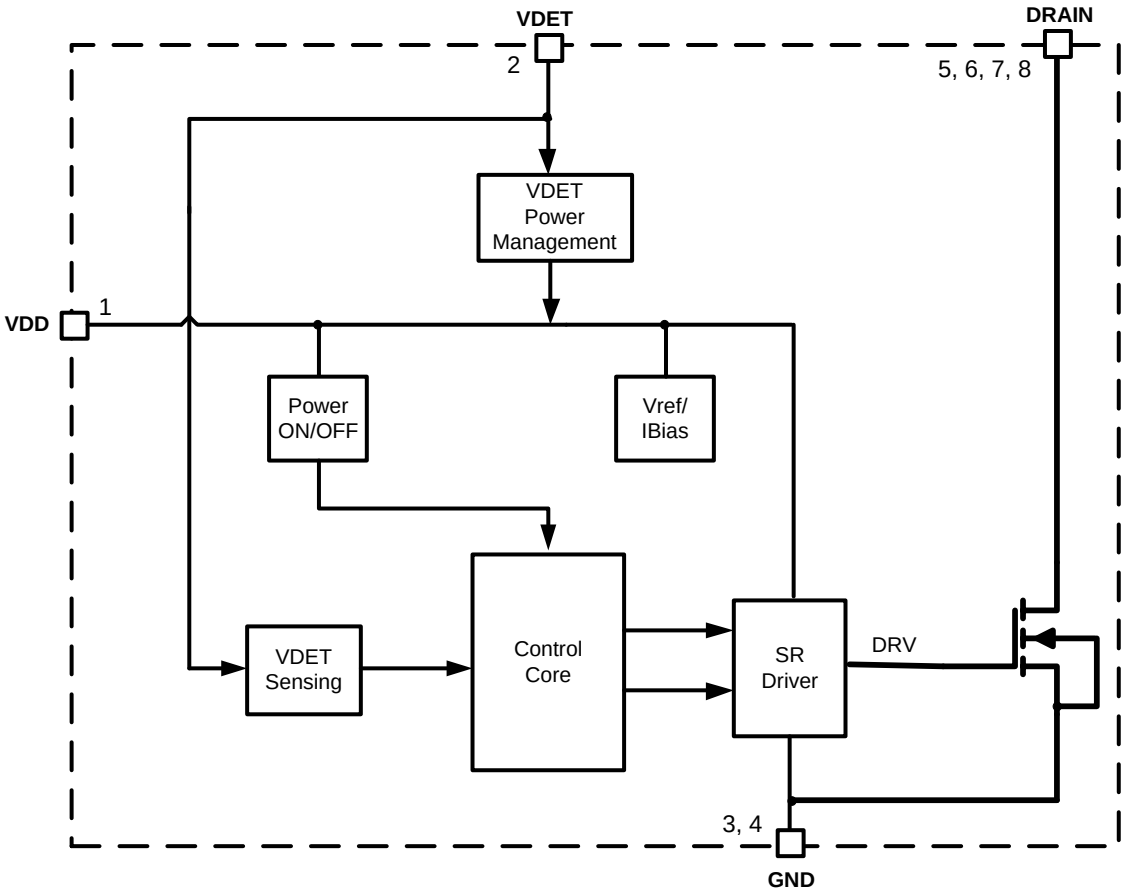
Low Side

High Side

Pin Descriptions

Pin Number	Pin Name	Function
1	VDD	Supply input. It provides bias voltage for the internal logic circuit and the MOSFET driver.
2	VDET	MOSFET drain sensing
3,4	GND	Ground, also used as FET source sense reference for DRAIN
5, 6, 7, 8	DRAIN	Synchronous rectification MOSFET drain voltage sense input

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{DD}	Voltage at VDD Pin	-0.3 to 7	V
V_{DRAIN}, V_{VDET}	Voltage at DRAIN Pin and VDET pin	-0.7 to 100	V
P_D	Power Dissipation at T_A = +25°C	0.6	W
T_J	Operating Junction Temperature(Note 6)	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	78	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	7	°C/W
ESD	Human Body Model	4000	V
	Charged Device Model	1500	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

5. Test condition: Device mounted on FR-4 substrate PC board, 1mm width, 20mm length, 2oz power lead.

6. Setting +85°C in the aging condition.

Electrical Characteristics (@ V_{OUT} = 5V, T_A = -40°C <T_A< +85°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Internal Supply Section (VDD Pin)						
V_{DD_ON}	VDD ON Threshold Voltage	—	3.55	3.75	3.95	V
V_{DD_OFF}	VDD Off Threshold Voltage	—	3.35	3.55	3.75	V
V_{DD_REG}	VDD Regulation Voltage	V_{OUT} = 3V, V_{DRAIN} = 12V	5.3	5.7	6.5	V
I_{Q_VDD}	Quiescent Current	V_{DD} = 5.0V	—	190	255	μA
MOSFET Section (VDET Pin)						
V_{ON_TH}	Turn-On Threshold Voltage	Voltage at VDET Pin	-225	-200	-175	mV
V_{ON_REG}	Turn-On Regulation Voltage(Note 7)	Voltage at VDET Pin	—	-40	—	mV
V_{ON_OFF}	Turn-Off Threshold Voltage(Note 7)	Voltage at VDET Pin	—	-7	—	mV
I_{CHG_VDD}	VDET to VDD Maximum Charging Current	—	50	—	105	mA
Control Section						
t_{ON_MIN}	GATE Minimum On Time	—	0.60	0.9	1.2	μs
t_{D_ON}	Turn-On Delay(Note 7)	C_{LOAD} = 2.2nF	—	30	—	ns
t_{D_OFF}	Turn-Off Propagation Delay(Note 7)	—	—	15	—	ns

Note: 7. Guaranteed by design.

Electrical Characteristics (continued)

MOSFET Static Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DSS(BR)}$	Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 0.25mA	100	—	—	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	—	—	0.4	μA
$R_{DS(ON)}$	Drain to Source On-state Resistance	V_{GS} = 4.5V, I_D = 2A	—	10	—	mΩ
V_{SD}	Diode Forward Voltage	V_{GS} = 0V, I_S = 2A	—	0.7	1.1	V
t_{RR}	Body Diode Reverse Recovery Time	I_F = 20A, di/dt = 100A/μs	—	44.3	—	ns
Q_{RR}	Body Diode Reverse Recovery Charge	I_F = 20A, di/dt = 100A/μs	—	65.5	—	nC

MOSFET Dynamic Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz	—	2309	—	pF
C_{oss}	Output Capacitance		—	536	—	
C_{rss}	Reverse Transfer Capacitance		—	13.7	—	
Q_{gs}	Gate to Source Charge	V_{DD} = 50V, I_D = 20A	—	7.0	—	nC
Q_{gd}	Gate to Drain Charge (Miller Charger)		—	8.5	—	
Q_g	Total Gate Charge	V_{GS} = 4.5V	—	20.2	—	
R_g	Gate Resistance	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz	—	1.9	—	Ω

Operation Description

VDD Regulator and UVLO Protection

The VDD is supplied by PLR (Pulse Linear Regulator) from the drain voltage. The APR34910 can be charged by internal PLR (Pulse Linear Regulator) at low system output voltage as low as 0V.

When VDD provides bias voltage for the controller. A capacitor (typical 3.3μF) should be connected between the VDD pin and GND pin. The APR34910 also has UVLO protection. When V_{DD} drops below V_{DD_UVLO}, the IC will stop providing gate drive pulse.

GATE Turn-On Logic

The APR34910 determines the synchronous rectification MOSFET turning-on time by monitoring the MOSFET drain-to-source voltage. When the drain voltage is lower than the turn-on threshold voltage V_{ON_TH}, the IC outputs a positive drive voltage after a turn-on delay time (t_{D_ON}). The MOSFET will then turn on and the current will transfer from the body diode into the MOSFET's channel.

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GATE Voltage Regulation/Auto-Tracking

A minimum on-time (t_{ON_MIN}) blanking period aims to prevent accidental turn-off due to interference of ringing noise voltage. When the controlled MOSFET gate turns on, some ringing noise will be generated. Utilizing a minimum on-time timer to blank the V_{THOFF} comparator keeps the SR MOSFET on for at least the minimum on-time. During this period, the gate driver can still be quickly pulled down to zero when the V_{DRAIN} ringing voltage goes over 2V.

Once the synchronous rectification gate outputs a high level voltage, the secondary-side current goes through synchronous rectification MOSFET. The voltage dropping on the MOSFET is calculated by $R_{DS(ON)}$ × secondary-side current. After minimum turn-on time t_{ON_MIN}, the IC continuously monitors V_{DRAIN} by the DRAIN pin and generates a pull-down current from the MOSFET gate until drain voltage equals to -40mV. As shown in Figure 1, the MOSFET drain-to-source voltage would remain around -40mV (V_{ON_REG}) with the secondary-side current decreasing.

Operation Description (continued)

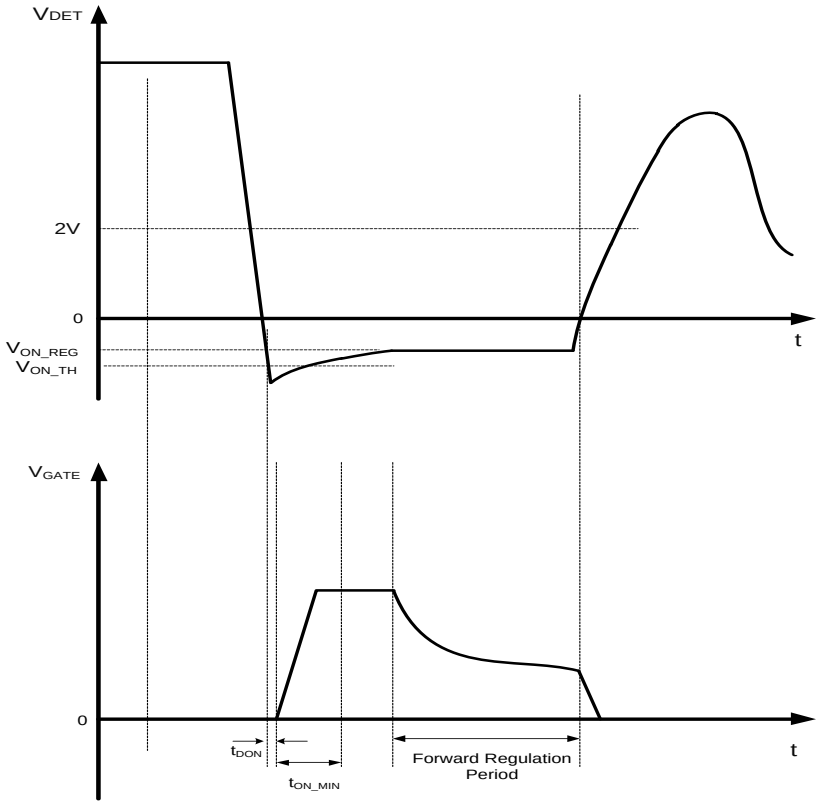


Figure 1. Forward Regulation Operation Principle

Smart-Blanking Control

Because of the resonance oscillation of primary inductance and equivalent output capacitance of the switching device, the voltage on the MOSFET drain pin has an under-damped voltage ring in DCM operation mode. In special occasions, such as output transition period or light-load conditions, the ring of the V_{DRAIN} will meet conduction requirement and the SR MOSFET will turn on falsely during the Toff period. When the turn–on of the primary MOSFET meets the false turn-on of the SR, there will be an immediate shoot-through of the transformer. To avoid such faults, the device utilizes a built-in smart-blanking function to prevent continuous false turn-on. When detecting false turn-on at least twice during a period of 4μs in the Toff time period, the SR gate driver will be blanked for a period of 20μs. Figure 2 shows the smart-blanking control method.

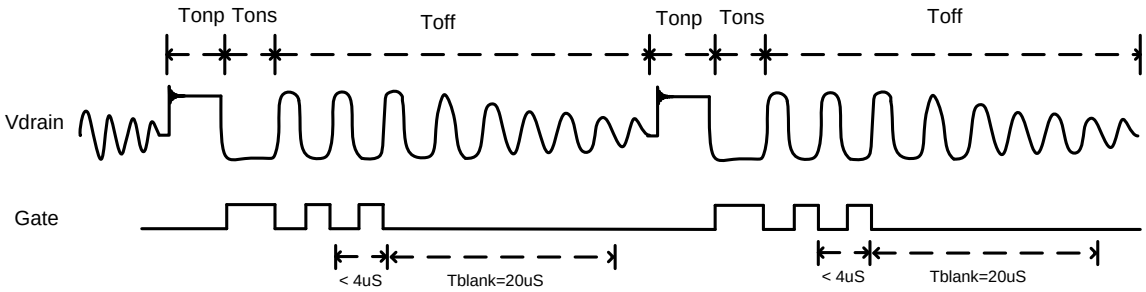
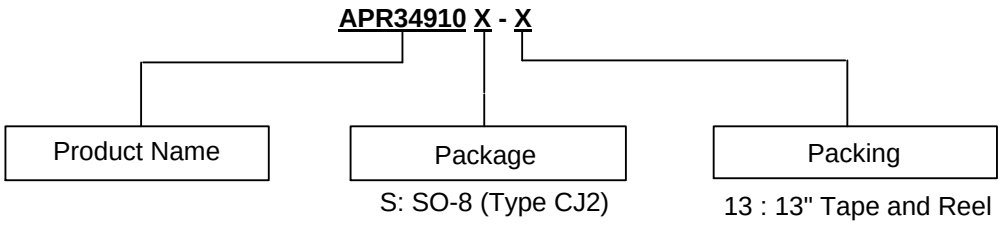


Figure 2. Smart-blanking Control Method

GATE Turn-Off Logic

When the V_{DRAIN} rises to the turn-off threshold (-7mV), the synchronous rectification MOSFET gate voltage will be quickly pulled down from a low voltage to zero after a very short turn-off delay. For CCM mode, when the primary MOSFET turns on, the secondary V_{DRAIN} will rise up in the meantime. Once drain voltage rises to the turn-off threshold, the gate-driving signal will be immediately shut down.

Ordering Information

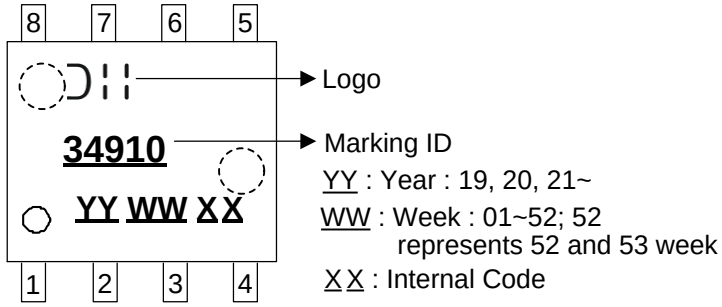


Package	Temperature Range	Part Number	Marking ID	13''Tape and Reel	
				Quantity	Part Number Suffix
SO-8 (Type CJ2)	-40 to +85°C	APR34910S-13	34910	4000/Tape and Reel	-13

Marking Information

SO-8 (Type CJ2)

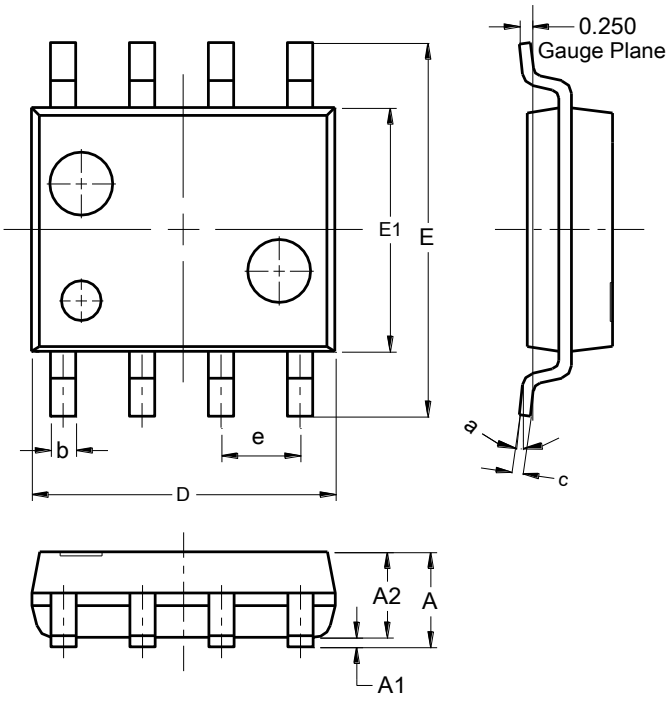
(Top View)



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8 (Type CJ2)

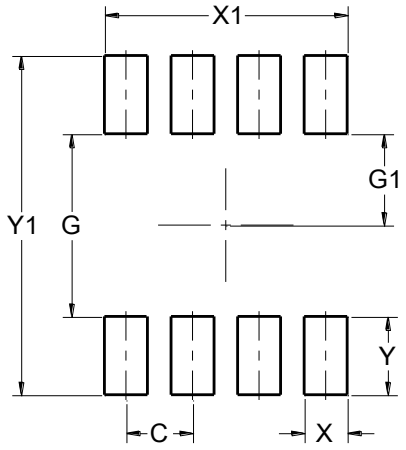


SO-8 (Type CJ2)			
Dim	**Min**	**Max**	**Typ**
A	1.450	1.750	--
A1	0.100	0.250	--
A2	1.350	1.550	--
b	0.330	0.510	--
c	0.170	0.250	--
D	4.700	5.100	--
E	5.800	6.200	--
E1	3.800	4.000	--
e	1.27 BSC		
L	0.400	1.270	--
A	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8 (Type CJ2)



Dimensions	Value (in mm)
C	1.270
G	3.500
G1	1.750
X	0.820
X1	4.630
Y	1.500
Y1	6.500

Mechanical Data

- Moisture Sensitivity: MSL Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.078719 grams (Approximate)

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